(Pages : 3) **9719**

Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, January 2016
(2013 Scheme)
13.305 : DIGITAL SYSTEM DESIGN (FR)

Time: 3 Hours Max. Marks: 100

PART – A

Answer for **all** questions. **Each** question carries **2** marks :

1. Write the canonical POS expression for the given function, $f(x_1, x_2, x_3) = \pi M(0,1,5)$.
2. Implement the given function by using NAND only circuit, $f(x_1, x_2, x_3) = \Sigma m(2, 3, 4, 6, 7)$.
3. Realize a XOR gate with NAND gates only.
4. Realize a D Flip Flop and T-Flip Flop with a JK Flip Flop.
5. What is race around condition for JK Flip Flop ?
6. Why the state diagram is necessary for simplification of a sequential circuit ?
7. Give the limitations of asynchronous counter.
8. Give the syntax for input array declaration using VHDL.
9. How the signed binary numbers are represented ?
10. Perform $0.101 \times 2^3 + 0.111 \times 2^5 = ?$ **(10×2=20 Marks)**

P.T.O.

PART – B

Answer **any one** question from **each** Module. **Each full** question carries **20** marks :

Module – I

11. a) Reduce the expression $S = \Sigma m\,(1, 2, 4, 6, 9, 11, 15) + d\,(3, 10, 14)$ by using a four variable K-map method. **14**

    b) Simplify the given Boolean functions using Boolean algebra and implement the same using logic gates :

    i) $Y = AB + A\,(B + C) + B\,(B + C)$

    ii) $Y = (A + B + C) \cdot (B + C) \cdot (A + C)$. **6**

OR

12. a) Simplify $P = \pi\,(0, 1, 2, 3, 8, 9, 11, 13, 15)$ using K-map and implement the circuit using logic gates. **12**

    b) Design and draw a full subtractor circuit using logic gates. **8**

Module – II

13. a) Reduce the given state table for minimum state, then find the output sequence generated with an input sequence of '0111001001'. Start from the state 'A' : **12**

Present State	Next State		Output	
	X = 0	X = 1	X = 0	X = 1
A	A	E	0	0
B	C	B	0	1
C	A	F	0	0
D	C	B	0	1
E	F	E	0	0
F	A	F	0	0
G	F	G	0	1

b) Explain carry look-ahead adder with the help of a block diagram. 8

OR

14. a) Draw the circuit of master slave flip and explain its mode of operation. 12

b) What is multiplexer ? Derive a logic diagram for a 8 : 1 multiplexer. 8

Module – III

15. a) Draw the logic circuit of a mod-10 BCD synchronous counter and explain the operation with the help of a timing diagram. 10

b) Write a VHDL code for realizing 4 : 1 multiplexer. 10

OR

16. a) What is the difference between Programmable Logic Device (PLD), Programmable Logic Array (PLA) and Programmable Array Logic (PAL) ? Explain with the help of diagrams. 15

b) The capacity of a 4K × 8 ROM is to be expanded to 16K × 8. Find the number of chips required and the number of address lines in the expanded memory. 5

Module – IV

17. a) Give the Shift and Add algorithm for performing 2 four bit binary multiplication. 10

b) Draw the block diagram for an unsigned binary numbers that divides an 8-bit dividend by a 3-bit divisor to give a 5-bit quotient. 10

OR

18. a) Explain the 2's complement algorithm for multiplying signed binary numbers with the help of a state graph. 15

b) Give the state diagram for a divider control circuit. 5